Amendments to the Claims

This listing of claims will replace all prior versions, and listings, of claims in the application:

RCE 6/3/04 filed ⇒ Enter Amendt. 3/1/04. M.T

All claims 1-12

Listing of Claims

1. (Currently Amended) A method of fabricating a NAND-type flash memory device, comprising:

forming a plurality of isolation layers running parallel with each other at predetermined regions of a semiconductor substrate;

forming a string selection line pattern~~, a plurality of word line patterns~~ and a ground selection line pattern crossing over active regions between the plurality of isolation layers ~~and active regions between the plurality of isolation layers~~, the string selection line pattern and the ground selection line pattern running parallel with each other;

forming a plurality of word line patterns disposed between the string selection line pattern and the ground selection line pattern;

ion-implanting impurities into the active regions among the string selection line pattern, the plurality of word line patterns and the ground selection line pattern, thereby forming drain regions at the active regions adjacent to the string selection line pattern and opposite the ground selection line pattern and concurrently forming source regions at the active regions adjacent to the ground selection line pattern and opposite the string selection line pattern;

forming a first interlayer insulating layer on the entire surface of the substrate including the drain and source regions;

patterning the first interlayer insulating layer to form a slit-type common source line contact hole exposing the source regions and the isolation layers between the source regions; and

forming a common source line filling the common source line contact hole~~;~~

~~wherein a top surface level of the common source line is even with or lower than a top~~